

CLAIM LISTING

1. (Currently Amended) A method for displaying a picture, said method comprising:

providing a first parameter to a first register indicating that the picture comprises a first number of lines, wherein the first parameter is determined by setting the first parameter to a line number associated with a desired line for repeating;

providing a second parameter to a second register, indicating that the picture comprises a second number of lines, wherein the second parameter is determined by setting the second parameter to a number of lines to be displayed;

receiving horizontal synchronization pulses;

providing the particular one of the first number of lines for scaling or composing or capturing for the horizontal synchronization pulses that are associated with particular ones of the first number of lines; and

repeatedly providing a last of the first number of lines for scaling or composing or capturing for each of the horizontal synchronization pulses that are associated with line numbers that exceed the first number of lines, from memory addresses, wherein the last of the first number of lines is provided from the same memory addresses during each repetition.

2. (Cancelled)

3. (Previously Presented) The method of claim 2, further comprising:

if the horizontal synchronization pulse is associated with a particular one of the first number of lines, fetching the particular one of the first number of lines for scaling or composing or capturing; and

if the horizontal synchronization pulse is not associated with a particular one of the first number of lines, fetching a last of the first number of lines for scaling or composing or capturing.

4. (Currently Amended) A decoder system for displaying a picture, said decoder comprising:

a feeder for fetching lines of the picture;

a scalar for scaling lines of the picture;

a compositor composing multiple video/graphics layers;

a video capture capturing the picture into DRAM and

a controller for providing a first parameter to the feeder indicating that the picture comprises a first number of lines and providing a second parameter to the scalar or compositor or capture indicating that the picture comprises a second number of lines, wherein the first parameter is determined by setting the first parameter to a line number associated with a desired line for repeating and wherein the second parameter is determined by setting the second parameter to a number of lines to be displayed; and

wherein the feeder repeatedly fetches the desired line for repeating from the same memory addresses during each repetition.

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5. (Original) The decoder system of claim 4, wherein the feeder comprises a register for storing the first parameter and wherein the scalar or compositor or capture comprises a register for storing the second parameter.

6. (Cancelled)

7. (Previously Presented) The decoder system of claim 4, wherein the scalar or compositor or capture receives horizontal synchronization pulses, and wherein the feeder provides the particular one of the first number of lines for scaling or composing or capturing for the horizontal synchronization pulses that are associated with particular ones of the first number of lines and repeatedly provides a last of the first number of lines for scaling or composing or capturing for each of the horizontal synchronization pulses that are associated with line numbers that exceed the first number of lines.

8. (Original) The decoder system of claim 7, wherein the feeder fetches a particular one of the first number of lines for scaling or composing or capturing that is associated with the horizontal synchronization pulse, if the horizontal synchronization pulse is associated with any of the first number of lines and fetches a last of the first number of lines for scaling or composing or capturing if the horizontal synchronization pulse is not associated with any of the first number of lines.

9. (Currently Amended) A circuit for displaying a picture, said circuit comprising:

a feeder;

a scalar connected to the feeder;

a compositor connected to the feeder;

a video capture connected to the feeder; and

a controller connected to the feeder, the scalar, the compositor, the capture and the controller operable to program a feeder with a first parameter indicating that the picture comprises a first number of lines and program a scalar or compositor or capture with a second parameter indicating that the picture comprises a second number of lines, wherein the first parameter is determined by setting the first parameter to a line number associated with a desired line for repeating and wherein the second parameter is determined by setting the second parameter to a number of lines to be displayed; and

wherein the feeder is operable to repeatedly fetch the desired line for repeating from the same memory addresses during each repetition.

10. (Original) The circuit of claim 9, further comprising:

memory connected to the controller, said memory storing a plurality of instructions, wherein execution of the plurality of instructions by the controller causes:

programming the feeder with the first parameter indicating that the picture comprises a first number of lines; and

programming the scalar or compositor or capture with the second parameter indicating that the picture comprises a second number of lines.

11. (Original) The circuit of claim 9, the feeder comprising a register storing the first parameter, the scalar or compositor or capture comprising a register storing the second parameter, and the controller operable to write the first parameter to the first register and the second parameter to the second register.

12. (Original) The circuit of claim 11, wherein the scalar or compositor or capture receives a horizontal synchronization pulse and is operable to request a line of the picture associated with the horizontal synchronization pulse.

13. (Original) The circuit of claim 12, wherein the feeder is operable to provide a particular one of the first number of lines for scaling that is associated with the horizontal synchronization pulse, if the horizontal synchronization pulse is associated with any of the first number of lines and provide a last of the first number of lines for scaling or composing or capturing if the horizontal synchronization pulse is not associated with any of the first number of lines.

14. (Original) The circuit of claim 13, wherein the feeder is operable to fetch a particular one of the first number of lines for scaling that is associated with the horizontal synchronization pulse, if the horizontal synchronization pulse is associated with any of the first number of lines and fetch a last of the first number of lines for scaling or composing or capturing if the horizontal synchronization pulse is not associated with any of the first number of lines.

15. (New) The method of claim 1, wherein the first number and the second number indicate a number of luma lines.